ELECTRONIC CIRCUITS I EE338

INDEX

BASICS

Voltage Gain:

$$A_v = \frac{v_O}{v_I}$$
$$A_{v(dB)} = 20\log|A_v|$$

A_v = voltage gain [V/V]
v_O = output voltage [V]
v_I = input voltage [V]
$A_{v(dB)}$ = voltage gain [decibels]

Power Gain:

$$A_p = \frac{P_L}{P_I} = \frac{v_O\, i_O}{v_I\, i_I} = A_v A_i$$
$$A_{p(dB)} = 10\log A_p$$

A_p = power gain [W/W]
P_L = load power [W]
P_I = input power [W]
$A_{p(Db)}$ = power gain [decibels]

Current Gain:

$$A_i = \frac{i_O}{i_I}$$
$$A_{i(dB)} = 20\log|A_i|$$

A_i = current gain [I/I]
i_O = output current [I]
i_I = input current [I]
$A_{i(\mathrm{dB})}$ = current gain [decibels]

When the gain A_v or A_i is negative it means there is a 180° phase shift between input and output. When a gain expressed in decibels is negative, it means the signal is attentuated.

Efficiency:

$$\eta \equiv \frac{P_L}{P_{\mathrm{dc}}}$$
$$P_{\mathrm{dc}} + P_I = P_L + P_{\mathrm{dissipated}}$$

P_L = load power [W]
P_{dc} = power supplied [W]
P_I = input power [W]

If a circuit is **linear**, it means it can be described by linear equations (no exponents).

AC-DC NOTATION CONVENTIONS:

$$v_B = V_B + v_b$$

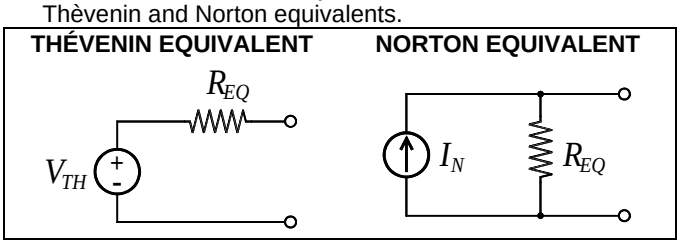
v_B = total voltage [V]
V_B = DC voltage [V]
v_b = AC (signal) voltage [V]

UNITS CONVENTION

For this class, currents were in terms of **mA** and resistances were in term of **k**W.

THÈVENIN AND NORTON EQUIVALENTS

A **one-port network** (circuit presenting 2 external terminals) may be represented by either a Thèvenin or Norton equivalent. Note that R_{EQ} has the same value in both the Thèvenin and Norton equivalents.



The Thèvenin voltage V_{TH} is the open-circuit voltage.

The Norton current I_N is the short-circuit current.

It is only necessary to find one or the other. If there are no independent sources (dependent sources may be present) then $V_{TH} = I_N = 0$ and the circuit reduces to an equivalent resistance.

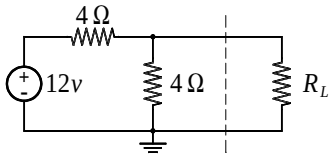
To find R_{EQ}:

1) "Turn off" the independent sources, i.e. voltage sources go to zero which means they are shorted and current sources also go to zero which means they are opened.
2) If there are independent and dependent sources, turn off the independent sources and apply a test source (V_{TEST} = 1 or I_{TEST} = 1) to the port. Calculate the unknown parameter V_{TEST} or I_{TEST} at the port and find R_{EQ} using

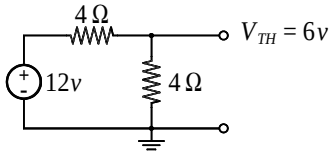
$$V_{TEST} = I_{TEST} R_{EQ}$$

THÈVENIN/NORTON EXAMPLE

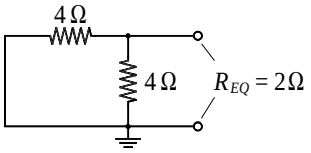
Given this circuit:



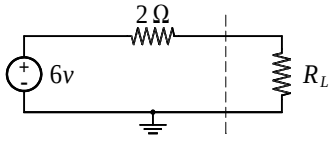
The Thèvenin voltage is the open circuit voltage, i.e. with the load disconnected.



The Thèvenin resistance is the equivalent resistance with the independent voltage source shorted and the load disconnected.

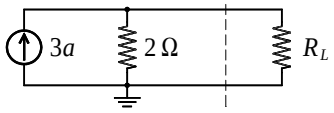


The Thèvenin equivalent circuit can now be written as:



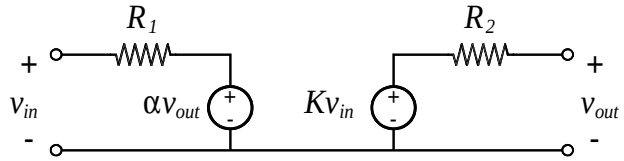
$$V_{TH} = I_N R_{TH}$$

And the Norton equivalent can be written as:

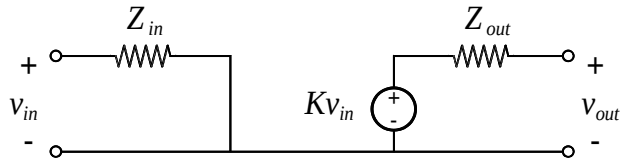


2-PORT LINEAR NETWORKS

All may be described by (4 variables: R_1, R_2, K, α):



If α is close to zero, we can use (3 variables: Z_{in}, Z_{out}, K):

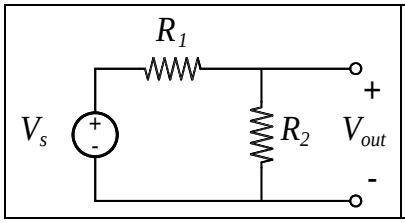


PARALLEL RESISTANCE

$$R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

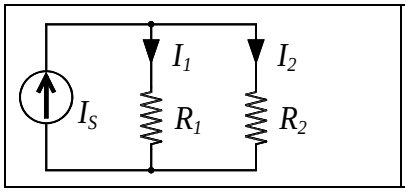
$$R_1 \parallel R_2 \parallel \cdots \parallel R_N = \frac{1}{R_1^{-1} + R_2^{-1} + \cdots R_N^{-1}}$$

VOLTAGE DIVISION



$$V_{out} = \frac{R_2}{R_1 + R_2} V_s$$

CURRENT DIVISION

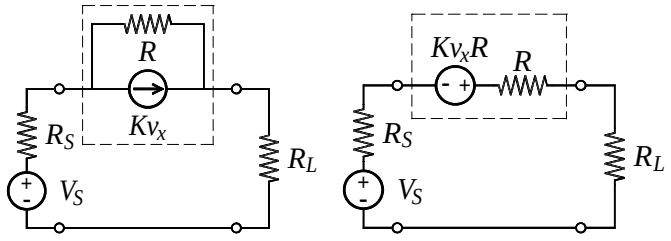


$$I_1 = \frac{R_2}{R_1 + R_2} I_S$$

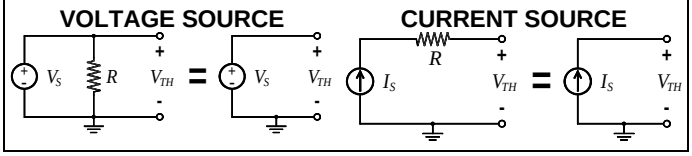
$$I_2 = \frac{R_1}{R_1 + R_2} I_S$$

SHORTCUTS AND TRICKS:

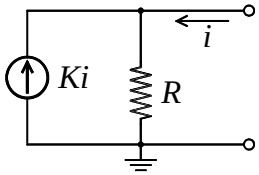
The circuit is simplified by recognizing a Norton equivalent and converting to a Thévenin equivalent.



A resistance in parallel with a voltage source or in series with a current source may be eliminated.



When a dependent current source and the current on which it depends both feed into a resistor as shown, the two components may be replaced by a single resistance R_{EQ} calculated as follows:

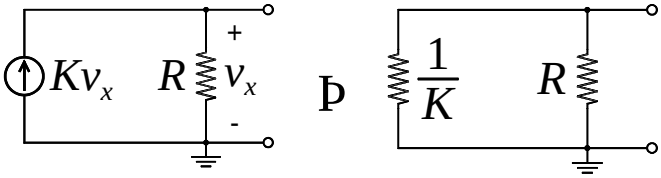


$$R_{EQ} = (K+1)R$$

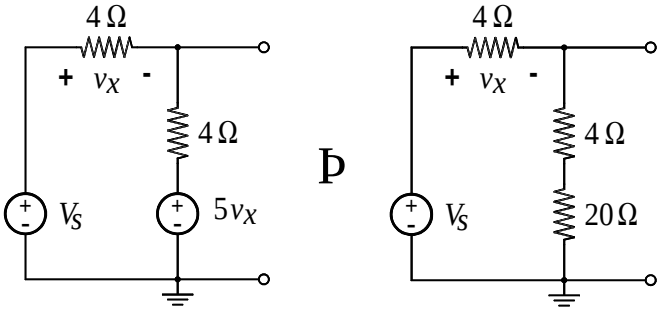
If the direction of i was reversed then

$$R_{EQ} = (K-1)R$$

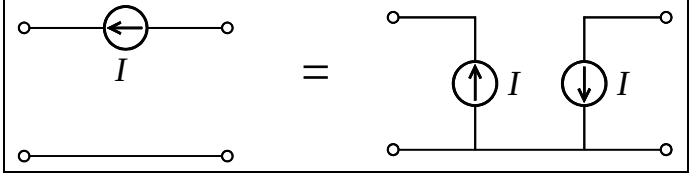
When a current source is dependent on the voltage across itself, it may be replaced by a resistor equal to the inverse of the current source's coefficient:



A dependent voltage source may be replaced with a resistor providing the same voltage drop in order to find V_{TH}. However, this **cannot** be used to find R_{EQ}.

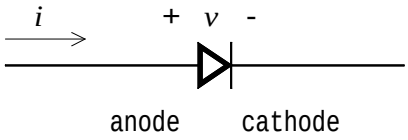


A current source may be rerouted to another point provided a second source of equal magnitude is created with flow from that point to the original. I may be independent or dependent.



DIODES

FORWARD-BIASED DIODE



CHARACTERISTICS OF THE IDEAL DIODE

- If v is negative, the diode is *reversed biased* and acts as a closed switch with $v = 0$.
- If a positive current is applied in the direction shown, the diode is *forward biased* and acts like an open circuit.

CHARACTERISTICS OF A REAL DIODE

- If v is negative, the diode is *reversed biased*. If the magnitude of v is small, the diode conducts little until the magnitude of v reaches the *breakdown voltage* at which point the diode conducts.
- If a positive current is applied in the direction shown, the diode is *forward biased*. There is not a significant amount of conduction until the voltage reaches about 0.7V.

THE *I*:*V* RELATIONSHIP IN THE FORWARD-BIAS REGION

$$I_D = I_S(e^{V_D/nV_T} - 1)$$

The -1 is unimportant since the $e^{VD/nVT}$ term is on the order of 10^{12} so it is eliminated:

$$I_D = I_S\, e^{V_D/nV_T}$$

$$\ln(I_D / I_S) = V_D / nV_T$$

I_D = diode current
I_S = saturation current
e = natural number
V_D = voltage across diode
n = 1 generally
V_T = thermal voltage, ≈ 25 mV

SIGNAL ANALYSIS

The total signal is the AC signal plus the DC signal.
For AC signal analysis, turn off DC sources. Consider the diode as a resistance r_d.
For DC analysis, turn off AC sources.

$$r_d = \frac{nV_T}{I_D}$$

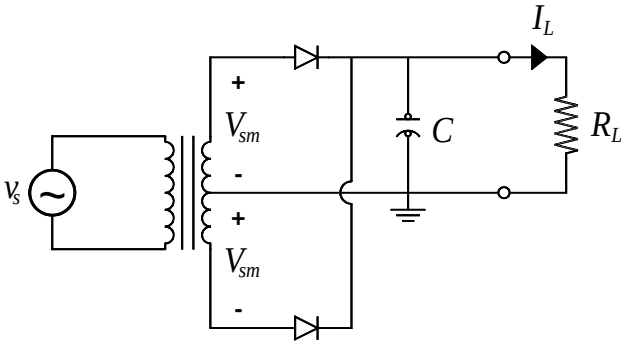
THERMAL VOLTAGE

$$V_T = \frac{kT}{q}$$

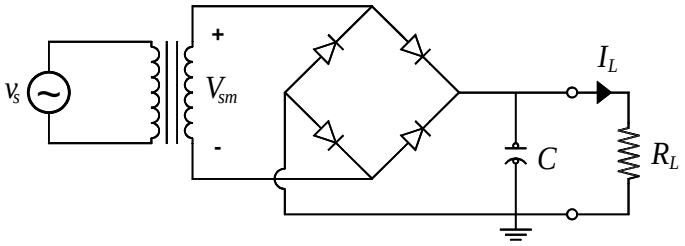
V_T = thermal voltage, ≈ 25 mV
k = Boltzmann's constant, 1.38×10^{-23} joules/kelvin
T = absolute temperature (kelvins), 273 + temp. in °C
q = magnitude of electronic charge, 1.60×10^{-19} coulomb

RECTIFIER CIRCUITS

2-DIODE FULL-WAVE RECTIFIER



FULL-WAVE BRIDGE RECTIFIER



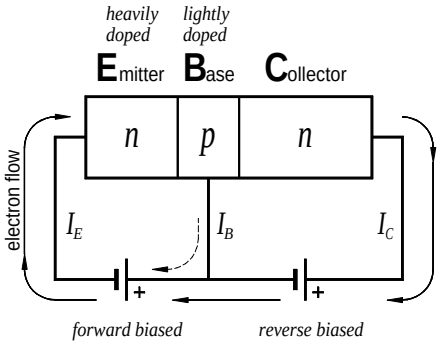
Formulas apply for small ripple voltages:

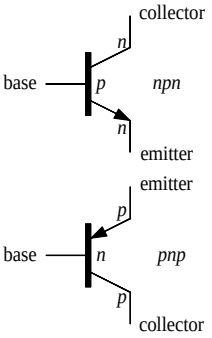
$$V_{ripple} = \frac{V_{sm}}{2\,fR_LC}$$

$$V_L = V_{sm} - \frac{V_{ripple}}{2}$$

V_{ripple} = ripple voltage, peak to peak
V_{sm} = transformer voltage, peak
f = frequency [Hz]
R_L = load resistance [Ω]
C = capacitance [F]

BIPOLAR JUNCTION TRANSISTORS - DC ANALYSIS



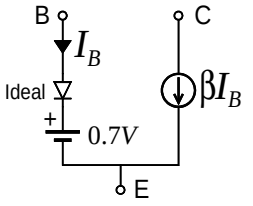


(Current flows in the direction of the arrow)

Bias: the difference in DC potential between base and emitter.

DC ANALYSIS MODEL (NPN)

For PNP, reverse the polarities of the diode and voltage supply. I_B and βI_B remain as shown but will have negative values.



***Q*-POINT:**

The *Q*-Point (also quiescent point, dc bias point, or operating point) is the center of the **transfer characteristic** (operating voltage range). It is adjusted by setting the DC voltage level of the base terminal.

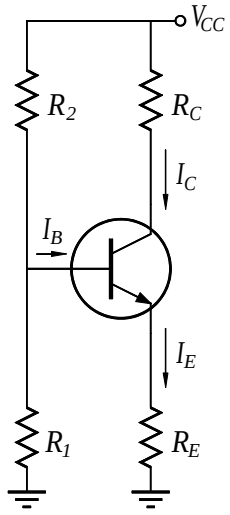
Rule of Thumb: To set the Q-Point, let

$$V_B = R_C I_C = \frac{1}{3} V_{CC}$$

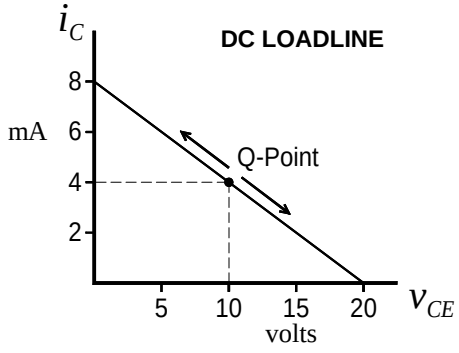
and

$$I_1 = 10 I_B = 10 \frac{I_E}{\beta + 1}$$

where I_1 is the current through the base-to-ground resistor.



A transistor amplifier is biased so that the ***Q*-Point** is located near the center of the **DC Loadline**. When an AC signal is applied, the *Q*-Point oscillates along the loadline.



BASE CURRENT:

The relationships among the emitter, base, and collector currents are functions of b. The relationships apply to signal current as well as DC current.

$$I_C = \beta I_B \qquad I_E = (\beta + 1) I_B$$

I_B = DC base current
I_C = DC collector current
I_E = DC emitter current
β = the **beta** value of the transistor

a **AND** b**:**

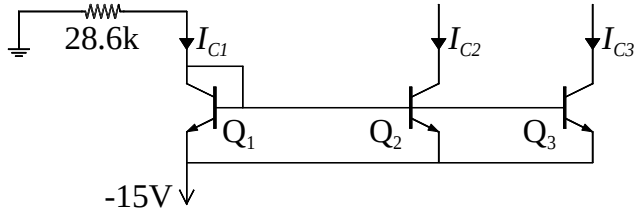
$$\alpha = \frac{I_C}{I_E} \qquad \beta = \frac{I_C}{I_B}$$

$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

a is constant for a particular transistor. It's value is less than but close to 1, normally 0.98-0.9995. a is the gain of a Common-Base amplifier.

b is constant for a particular transistor, typically in the range of 100 to 200 but may be 50-2000. Since the value of b may vary significantly among transistors of the same type, a b-tolerant circuit design is desirable. b is the Common-Emitter current gain.

CURRENT MIRROR



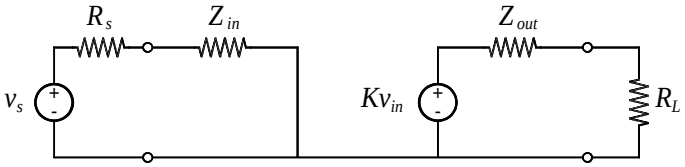
In this circuit, the base voltage is at -14.3V due to the 0.7V drop across the BE junctions. Since C_1 is also at -14.3V, I_{C1} will be ½mA. If all transistors are identical, then their base currents will be equal and $I_{C1} = I_{C2} = I_{C3} = ½mA$. Q_2 and Q_3 can be used as current sources to bias other transistors.

BIPOLAR JUNCTION TRANSISTORS - AC ANALYSIS

CIRCUIT LOADING

Loading is the loss of signal due to circuit resistance.

Some of the signal is lost in R_s; some output is lost in Z_{out}:



$$\text{gain} = \frac{v_{out}}{v_{in}} = K\,\frac{Z_{in}}{Z_{in}+R_s}\,\frac{R_L}{R_L+Z_{out}}$$

DETERMINING IMPEDANCE

TO FIND Z_{in}:

1) Remove the input source.
2) Leave the load connected.
3) Short other independent voltage sources; open other independent current sources.
4) If there are no dependent sources, the input impedance is determined by inspection, otherwise continue to step 5.
5) Keep in mind that current could flow in the circuit. Either a) manipulate the circuit using resistance reflection rule to ground out the independent sources, b) apply a test source to the input, or c) use other Tricks (p.2) to redraw the circuit.

TO FIND Z_{out}:

1) Remove the load .
2) Turn off the input source, but leave the source (resistance) connected.
3) Short other independent voltage sources; open other independent current sources.
4) If there are no dependent sources, the output impedance is determined by inspection, otherwise continue to step 5.
5) Keep in mind that current could flow in the circuit. Either a) manipulate the circuit using resistance reflection rule to ground out the independent sources, b) apply a test source to the output, or c) use other Tricks (p. 2) to redraw the circuit.

When calculating the gain, v_{out}/v_{in}, assume that sources and load (if shown) are connected.

EQUATIONS FOR AC ANALYSIS

@ room temperature:

$$\boxed{g_m = 40I_C} = \frac{I_C}{V_T}$$

$$\boxed{r_\pi = \frac{\beta}{g_m}} = \frac{\beta V_T}{I_C}$$

$$\boxed{r_o = \frac{V_A}{I_C}} \qquad \boxed{r_e = \frac{r_\pi}{\beta+1}}$$

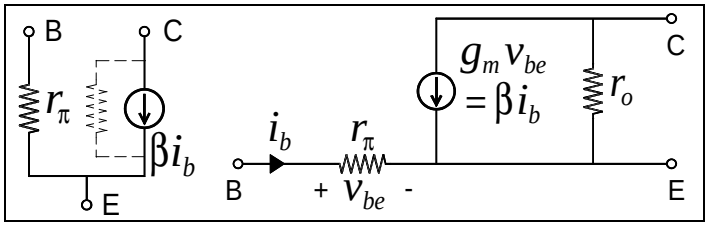
$$r_\pi \| \frac{1}{g_m} = r_e$$

g_m = transconductance [mA/V]
V_T = thermal voltage, ≈ 25 mV
I_C = collector current from DC analysis
V_A = a parameter of the particular BJT typically in the range of 50-100 volts, called the Early voltage

HYBRID p Small Signal Model for BJT Transistor

This works for PNP or NPN transistors without modification.

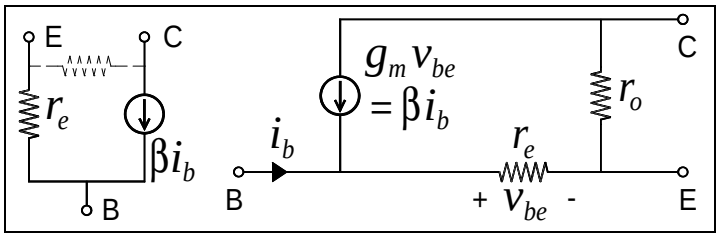
The same model is shown drawn 2 different ways. (r_o which is shown with dashed lines in the model at left, may usually be ignored.)



HYBRID T Small Signal Model for BJT Transistor

This works for PNP or NPN transistors without modification.

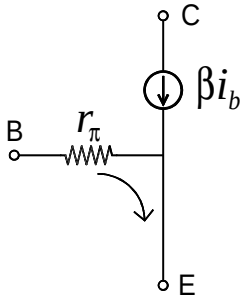
The same model is shown drawn 2 different ways. The T model is used if we can neglect r_o, that is r_o is very large.



RESISTANCE REFLECTION RULE

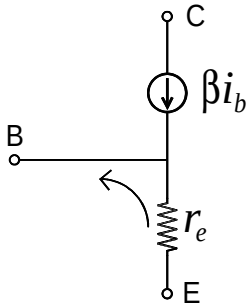
The **HYBRID** p and the **HYBRID T** models are again redrawn to illustrate conversion between the two:

HYBRID p Model



$$r_\pi \div (\beta+1) = r_e$$

HYBRID T Model



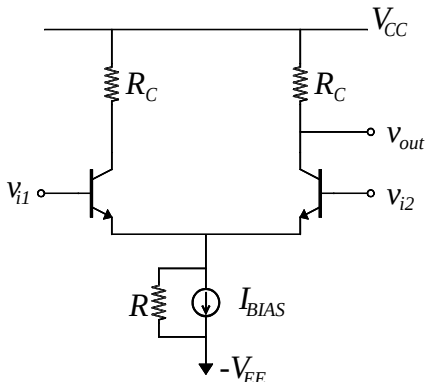
$$r_e \times (\beta+1) = r_\pi$$

One model is easily converted to the other. r_π is related to r_e by a factor of (β + 1). This has the effect of shifting the resistance between the base and emitter legs as shown above. A way to remember whether to multiply or divide is to know that base current is smaller than emitter current, so the base resistance must be larger. This is a powerful tool in AC analysis because other series resistances in the circuit may be combined with r_π or r_e and shifted with them.

DIFFERENTIAL AMPLIFIER ANALYSIS and BJT HIGH-FREQUENCY ANALYSIS

Differential amplifiers are used in integrated circuit design. In IC design, large capacitors and large (Ω) resistors are impractical. In this circuit, Q_2 eliminates the need to have a bypass capacitor to ground by providing a low-resistance path to signal ground.

SINGLE-ENDED OUTPUT DIFFERENTIAL AMPLIFIER



For AC analysis of differential amplifiers, we divide the input signals into differential and common-mode components. The inputs are written as

$v_{i1} = v_{icm} + \frac{v_{id}}{2}$	$v_{i2} = v_{icm} - \frac{v_{id}}{2}$

We solve for each separately using different models and then combine the results. For a description of the circuit analysis of the Single-Ended Output Differential Amplifier shown above, see the file **DifferentialAmplifierSEO.pdf.**

DIFFERENTIAL VOLTAGE GAIN

$$A_d = \frac{v_{od}}{v_{id}}$$

A_d = differential voltage gain [*V*/*V*]
v_{od} = total differential output voltage [*V*]
v_{id} = total differential input voltage [*V*]

COMMON-MODE VOLTAGE GAIN

$$A_{cm} = \frac{v_{ocm}}{v_{icm}}$$

A_{cm} = common-mode voltage gain [*V*/*V*]
v_{ocm} = common-mode output voltage [*V*]
v_{icm} = common-mode input voltage [*V*]

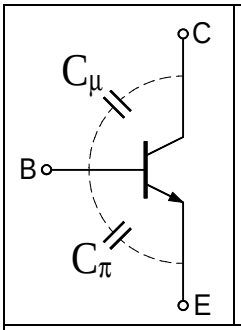
COMMON-MODE REJECTION RATIO (CMRR)

$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right|$$

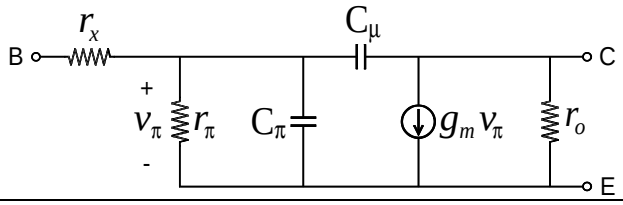
$$\text{CMRR}_{\text{dB}} = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right|$$

CMRR = common-mode rejection ratio. The ratio of the differential voltage gain to the common-mode voltage gain.
CMRR_{dB} = common-mode rejection ratio [decibels]

HIGH-FREQUENCY ANALYSIS

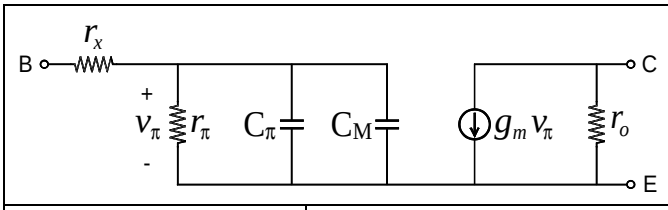


Small capacitances exist between the base and collector and between the base and emitter. These effect the frequency characteristics of the circuit.



THE MILLER EFFECT

The existance of C_μ complicates the above model. The Miller effect says that the model can be approximated by removing C_μ and replacing it with another gate-to-source capacitance C_M. K is the voltage gain across C_μ (assuming that C_μ represents an open circuit).



$$K = \frac{v_C}{v_\pi}$$

$$C_M = (1-K)C_\mu$$

$$\omega_{p1} = \frac{1}{\tau_1} = \frac{1}{RC}$$

In this case, with input disconnected:

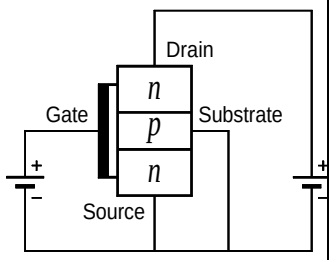
$$\tau_1 = r_\pi(C_\pi + C_M)$$

K = the voltage gain across C_m [*V*/*V*]
ω_{p1} = the input pole [rad/s]. Convert to Hz by dividing by 2π.
τ_1 = input time constant [seconds]
R = equivalent resistance [ohms]
C = input capacitance [farads]

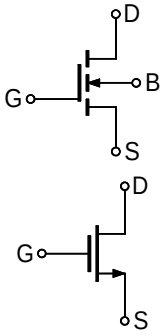
METAL OXIDE SILICON FIELD-EFFECT TRANSISTORS - *MOSFETs*

Enhancement MOSFET

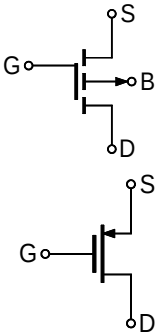
n-channel type: When a positive voltage is applied to the gate of the n-channel MOSFET shown at right, a channel of n material is formed within the p region near the gate. This enables current flow from drain to source. The substrate or base is usually internally connected to the source, forming a 3-terminal device.



n-channel (NMOS)



p-channel (PMOS)

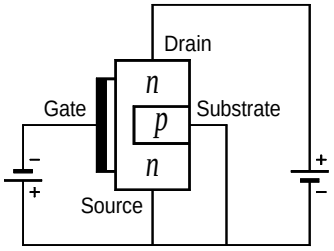


p-channel MOSFETs work like n-channel MOSFETs except all voltages are negative and current flows from S to D.

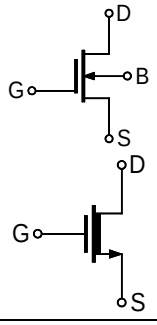
On 3-terminal devices, B is connected to D.

Depletion MOSFET

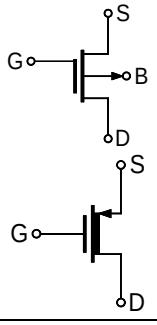
The n-channel Depletion MOSFET, as shown in the diagram at right, has an n-channel built in that allows current flow from drain to source. When a negative voltage is applied to the gate terminal, the channel becomes p material so that current flow is stopped.



n-channel (NMOS)



p-channel (PMOS)



In MOSFET circuits, there must be a resistor between gate and ground since the gate/substrate junction has a capacitance that can accumulate a destructive charge. The resistance should be high (around 1M) to preserve the high input impedance characteristic.

The Three Modes of Operation

CUTOFF - The region where the gate voltage is lower than the threshhold voltage V_t so that no current flows through the drain.

TRIODE - The region where v_{DS} is lower than the *excess gate voltage* and the characteristic curve is a curve. For small signals, the FET behaves like a voltage-controlled resistor. In the operating region, the characteristic curve may be thought of as a straight line, the slope of which is the inverse of the drain-to-source resistance.

SATURATION - The region where v_{DS} is greater than the *excess gate voltage* and the characteristic curve is a horizontal line. Drain current is a function of gate voltage v_{GS}. Drain current is constant (current saturated) with changes of v_{DS}.

THRESHHOLD VOLTAGE - V_t - the gate-to-source voltage at which an FET begins to conduct, usually 1 to 3 volts in an n-channel enhancement MOSFET.

EXCESS GATE VOLTAGE or **EFFECTIVE VOLTAGE** - The gate-to-source voltage in excess of the threshhold voltage, i.e. $v_{GS} - v_t$

ASPECT RATIO - W/L - the ratio of the channel width to the channel length (distance from source to drain).

CMOS (complementary MOS) - employing both n-channel (NMOS) and p-channel (PMOS) on the same chip.

GATE CAPACITANCE - The gate and substrate are separated by a thin, non-conducting metal oxide layer which causes the gate to act like a capacitor. It is necessary to connect a resistor between gate and ground to prevent a destructive charge from accumulating. The resistor should be on the order of 1 Meg to preserve the high impedance input characteristic.

DC DRAIN CURRENT

$$I_D = \frac{1}{2}k'\left(\frac{W}{L}\right)\left(v_{gs} - V_t\right)^2$$

This formula results in a quadratic equation with two answers. The lower value is the correct answer; or write an equation for v_{gs} and plug in values to see which works, i.e. $v_{gs} = v_g - v_s$.

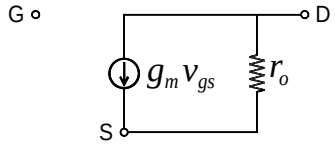
$$k' = \mu_n C_{ox}$$

W	is the channel width
L	is the channel length
v_{gs}	gate to source voltage
V_t	threshhold voltage
k'	is the process transconductance parameter [A/V^2]
μ_n	is the electron mobility in the channel. Typical value is 580 cm^2/Vs
C_{ox}	capacitance per unit area of the gate channel capacitance--permittivity of the silicon oxide divided by its thickness [F/m^2]

MOSFETs - AC ANALYSIS and FREQUENCY ANALYSIS

SMALL-SIGNAL MODELS

The circuit models for NMOS and PMOS FETs are the same. The arrow in the model's current source always points toward the FET's source terminal. This is the terminal of the circuit symbol which has an arrow, though the circuit symbol arrow may point either direction. The value of g_m is small and the value of r_o is large for FETs. This may affect what can be ignored.

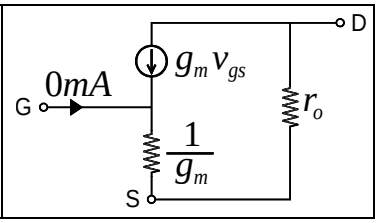


$$g_m = \sqrt{2k'(W/L)}\, I_D^{1/2}$$

$$r_o = \frac{V_A}{I_D}$$

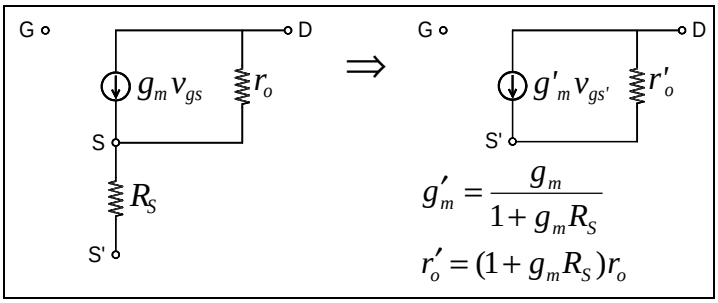
T-Model (seldom used)

Caution: Though it may not look like it, the input impedance is still infinity. No current flows through the gate.



SOURCE DEGENERATION

When a source resistance is present, it can be incorporated into the small-signal model, changing g_m, v_{gs}, and r_o. This is an approximation that assumes $g_m r_o >> 1$.

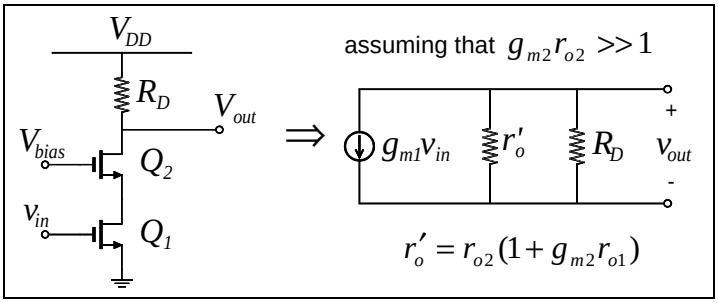


$$g'_m = \frac{g_m}{1 + g_m R_S}$$

$$r'_o = (1 + g_m R_S) r_o$$

CASCODE AMPLIFIER

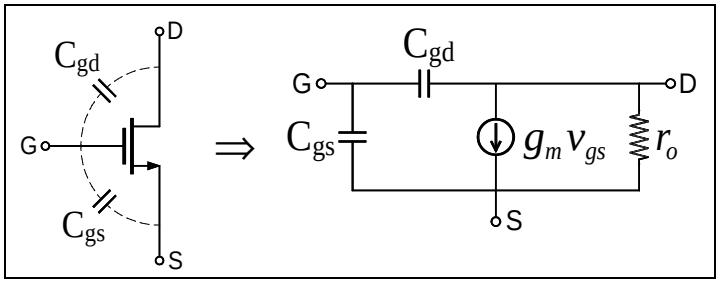
r_{01} acts as a degeneration resistance for Q_2, giving very high output impedance. The low impedance looking into the source of Q_2 guarantees that virtually all of the transconductance current $g_{m1}v_{in}$ of Q_1 will find its way to the load. Good high-frequency input characteristics. High output impedance.



$$r'_o = r_{o2}(1 + g_{m2} r_{o1})$$

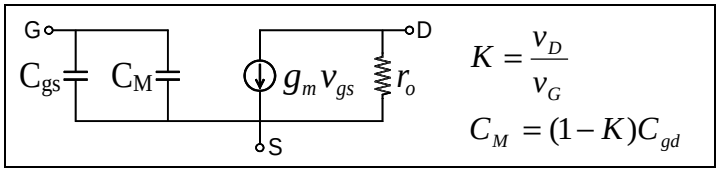
FREQUENCY ANALYSIS

Small capacitances exist between the gate and drain and between the gate and source. These effect the frequency characteristics of the circuit.



THE MILLER EFFECT

The existance of C_{gd} complicates the above model. The Miller effect says that the model can be approximated by removing C_{gd} and replacing it with another gate-to-source capacitance C_M. K is the voltage gain across C_{gd} (assuming that C_{gd} represents an open circuit).



$$K = \frac{v_D}{v_G}$$

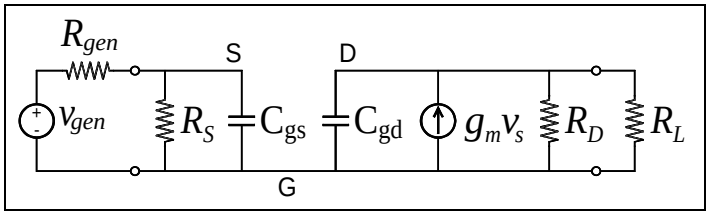
$$C_M = (1 - K) C_{gd}$$

THE POLES OF AN AMPLIFIER

$$\omega = \frac{1}{\tau} = \frac{1}{RC}$$

ω = the pole [rad/s]. Convert to Hz by dividing by 2π.
τ = time constant [seconds]
R = resistance [ohms]
C = capacitance [farads]

The poles of an amplifier are the frequencies at which the frequency response has dropped off by 3 dB, also called the *corner frequencies*. The CG model below has an input pole and an output pole.



INPUT POLE

$$\omega_1 = \frac{1}{RC} = \frac{1}{(R_{gen} \| R_S) C_{gs}}$$

(v_{gen} is turned off)

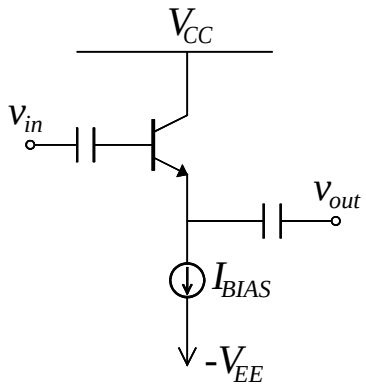
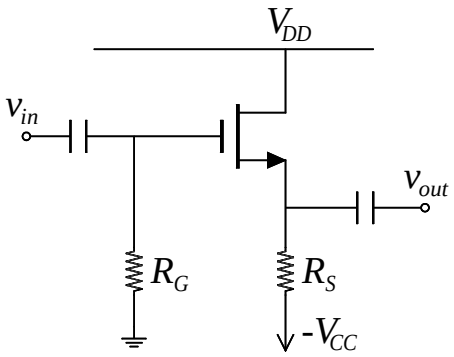
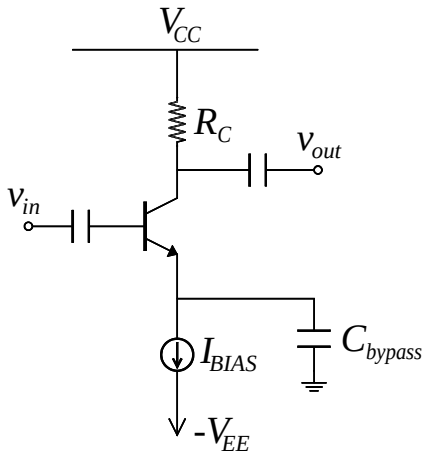
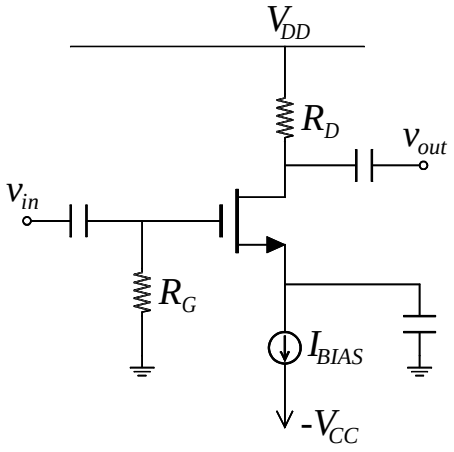
OUTPUT POLE

$$\omega_2 = \frac{1}{RC} = \frac{1}{(R_D \| R_L) C_{gd}}$$

EQUATION SUMMARY

	BJT	MOSFET
DC Current	$I_C = \beta I_B \qquad I_E = (\beta+1) I_B$	$I_D = \frac{1}{2} k' \left(\frac{W}{L}\right)\left(v_{gs} - V_t\right)^2$
Circuit Model Transconductance	$g_m = 40 I_C$	$g_m = \sqrt{2k'(W/L)}\, I_D^{1/2}$
Circuit Model Resistances	$r_\pi = \frac{\beta}{g_m} \qquad r_o = \frac{V_A}{I_C} \qquad r_e = \frac{r_\pi}{\beta+1}$	$r_o = \frac{V_A}{I_D}$
Differential Amplifier Gain and Common-mode Rejection Ratio	$A_d = \frac{v_{od}}{v_{id}} \qquad A_{cm} = \frac{v_{ocm}}{v_{icm}}$ $\text{CMRR} = \left\lvert\frac{A_d}{A_{cm}}\right\rvert \qquad \text{CMRR}_{\text{dB}} = 20\log_{10}\left\lvert\frac{A_d}{A_{cm}}\right\rvert$	
Source Degeneration Model		$g_m' = \frac{g_m}{1 + g_m R_S}$ $r_o' = (1 + g_m R_S)\, r_o$
Cascode Amplifier Model		$g_m' = g_{m1} \qquad R_D' = R_D$ $r_o' = r_{o2}(1 + g_{m2} r_{o1})$
Miller Effect	$K = \frac{v_C}{v_\pi} \qquad C_M = (1-K) C_\mu$	$K = \frac{v_D}{v_G} \qquad C_M = (1-K) C_{gd}$
Amplifier Poles or Corner Frequency	$\omega = \frac{1}{\tau} = \frac{1}{RC}$	

TYPES OF SINGLE-TRANSISTOR AMPLIFIERS

	BJT	MOSFET
Common Collector or Emitter Follower (BJT) **Common Drain or Source Follower (MOSFET)** High input impedance. --- • Current gain • Power gain • Low output impedance • Voltage gain is less than one • No Miller effect • Used as a buffer amplifier or output stage		
Common Emitter (BJT) Voltage gain is dependent on β. By adding a resistance at the emitter terminal, this dependence is reduced, input resistance is increased, voltage gain is reduced, and high-frequency response is improved. **Common Source (MOSFET)** High input impedance. Not subject to body effect --- • Current gain • Voltage gain • High output impedance • Suffer from the Miller Effect.		
Common Base (BJT) Voltage gain has little dependence on β. **Common Gate (MOSFET)** --- • Low input impedance. • Non-inverting. • Better at high frequencies. • Used in cascode amplifier